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08/17/02 Jc820 U.S. PTO

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. EV 073381557 US

INVENTOR(S)

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☐ *Additional inventors are being named on the _______ separately numbered sheets attached hereto*

Jc918 U.S. PTO

TITLE OF THE INVENTION (500 characters max)

METHODS FOR BARRIER AND SACRIFICAL LAYER REMOVAL

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ENCLOSED APPLICATION PARTS *(check all that apply)*

☑ Specification *Number of Pages* 7
☑ Drawing(s) *Number of Sheets* 4
☑ Application Data Sheet. See 37 CFR 1.76
☐ CD(s), Number ________
☑ Other (specify) RETURN RECEIPT POSTCARD

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☑ Applicant claims small entity status. See 37 CFR 1.27.
☑ A check or money order is enclosed to cover the filing fees
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☑ No
☐ Yes, the name of the U.S. Government agency and the Government contract number are ________

Respectfully submitted,

SIGNATURE ________ Date 8/17/02

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REGISTRATION NO *(if appropriate)* ________
Docket Number: ________

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Application Data Sheet

Application Information

Application Type::	Provisional
Subject Matter::	Utility
Suggested classification::	
Suggested Group Art Unit::	
CD-ROM or CD-R?::	
Number of CD disks::	
Number of copies of CDs::	
Sequence submission?::	
Computer Readable Form (CRF)?::	
Number of copies of CRF::	
Title::	Methods for Barrier and Sacrificial Layer Removal
Attorney Docket Number::	
Request for Early Publication?::	
Request for Non-Publication?::	
Suggested Drawing Figure::	
Total Drawing Sheets::	4
Small Entity?::	Yes
Petition included?::	
Petition Type::	

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Representative Designation::	Registration number::	Name::
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Domestic Priority Information

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METHODS FOR BARRIER AND SACRIFICAL LAYER REMOVAL

BACKGROUND

1. Field of the Invention

The present invention generally relates to semiconductor wafers. More particularly, the present invention relates to barrier removal and adding nonconductive sacrificial layer to improve barrier removal during polishing and plasma etching processes.

2. Background

In general, semiconductor devices are manufactured or fabricated on disks of semiconducting materials called wafers or slices. More particularly, wafers are initially sliced from a silicon ingot. The wafers then undergo multiple masking, etching, and deposition processes to form the electronic circuitry of semiconductor devices.

In recent years, the use of dielectric materials having low dielectric constants (low-k dielectrics) has been introduced in the semiconductor industry as the solution to reduce the signal delays at the interconnections of conductors, which connect elements of a single semiconductor device and/or connect any number of semiconductor devices together). However, because low-k dielectric materials have porous microstructures, they also have lower mechanical integrity and thermal conductivity than other dielectric materials. Consequently, low-k dielectric materials typically cannot sustain the stress and pressure applied to them during a conventional damascene process.

First in a conventional damascene process, multiple masking and etching are used to form recessed areas in a wafer, such as trenches, vias, and the like. Then metal is patterned within the trenches and/or via. Such process may include forming a barrier

layer over the metal or low-k dielectric materials. Deposition processes can be used to deposit metal onto the trenches and/or via, as well as non-recessed areas. The deposited metal is then typically polished back using chemical mechanical polishing (CMP), or electropolishing and the like, such that the metal from the non-recessed areas of the wafer is removed and the metal left in the trenches and/or vias can form interconnections.

Since barrier layer is usually formed by hard and chemical inert material such as TaN, Ta, Ti, and TiN, such barrier layer is difficult to remove using CMP or electropolish, except by using higher pad pressure during CMP or higher voltage during electropolishing. In the case of CMP, higher pad pressure will increase surface defect density, or even delaminate low-k dielectric. In the case of electropolishing, higher polishing voltage will remove copper, thus the copper line resistance will increase. When conventional plasma etching is used to remove barrier layer, over-etching is necessary in order to make sure all barrier layer on non-recessed area is removed. However, the over-etching will cause notch on barrier layer between copper and dielectric materials. Such notch will form a void when the next cover layer is deposited. Copper atoms can diffuse out from the void and can even diffuse to the device gate region, finally making semiconductor device malfunction.

Accordingly, adjusting the chemistry during the barrier removal or adding sacrificial layers during the masking process will eliminate voids from forming within the wafer.

DESCRIPTION OF THE DRAWING FIGURES

The present invention can be best understood by reference to the following detailed description taken in conjunction with the accompanying drawing figures, in which like parts may be referred to by like numerals:

Figs. 1A to 1D illustrate, in cross-sectional view, an exemplary damascene process;

Figs. 2A to 2D illustrate, in cross-sectional view, an exemplary damascene process, in accordance with the present invention;

Figs. 3A to 3D illustrate, in cross-sectional view, another exemplary damascene process, in accordance with the present invention; and

Figs. 4A to 4D illustrate yet again, in cross-sectional view, another exemplary damascene process, in accordance with the present invention.

DETAILED DESCRIPTION

In order to provide a more through understanding of the present invention, the following description sets forth numerous specific details, such as specific configurations, parameters, examples, and the like. It should be recognized, however, that such description is not intended as a limitation on the scope of the present invention, but is intended to provide a better description of the exemplary embodiments.

Fig. 1 depicts an exemplary damascene process that can be used to form interconnections in a semiconductor device. In particular, with reference to Fig. 1A, the semiconductor device can include a dielectric material 1008 having recessed area 1006 and non-recessed area 1007, where recessed area 1006 can be a structure such as a wide trench, a large rectangular structure, and the like. A barrier layer 1004 can be deposited on dielectric material 1008 by any convenient deposition method, such as a chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), and the like, such that barrier layer 1004 covers both recessed area 1006 and non-recessed area. For a more detailed discussion of dielectric material 1008 and barrier layer 1004, see U.S. Patent Serial No. 10,108,614, entitled ELECTROPOLISHING METAL LAYERS ON WAFERS HAVING TRENCHES OR VIAS WITH DUMMY STRUCTURES, filed on March 27, 2002, which claims priority of an earlier filed

provisional application U.S. Ser. No. 60/286,273, of the same title, filed on April 24, 2001. The entire content of both applications are incorporated herein by reference.

In the present exemplary process, metal layer 1009 can be deposited onto the barrier layer 1004 by any convenient method, such as PVD, CVD, ALD, electroplating, electroless plating, and the like, as shown in Fig. 1B. Next, deposited metal is polished back using CMP or electropolishing, and the like, such that the metal from the non-recessed area is removed and the metal is left in the recessed area 1006. As shown in Fig. 1C, metal layer can fill recessed area 1006 while the non-recessed area of barrier layer 1004 is bare of any deposited metal. As described in the co-pending application, metal layer can include various electrically conductive materials, such as copper, aluminum, nickel, chromium, zinc, cadmium, silver, gold, rhodium, palladium, platinum, tin, lead, iron, indium, super-conductor materials, and the like. Preferably, metal layer can include copper. Furthermore, it should be recognized that metal layer can include an alloy of any of the various electrically conductive materials, or compound of superconductor.

Now, with reference to Fig. 1D, after removing metal layer from non-recessed area, barrier layer 1004 can be removed from non-recessed area by any convenient method such as wet etching, dry chemical etching, dry plasma etching, and the like. In order to have all barrier layers on non-recessed area 1007 removed, usually over-etching is required. When applying over-etching, a notch 1010 as shown in Fig. 1D can occurs. When the next cover layer such as SiN and the like are deposited in the present exemplary process, notch 1010 can become a void, which can lead to copper bleeding. The bled copper can diffuse through dielectric material 1008 and down to the device gate region, causing the semiconductor device to malfunction.

In order to overcome this problem, as shown in Figs 2A – 2D, combination of overpolish using electropolish and plasma etching is disclosed here. In this exemplary process as shown in Fig. 2A, deposited metal in the recessed area 1006 is overpolished using electropolishing, or wet etching and like, so that there exists h micron in height between the top of the barrier layer 1004 and the surface of metal layer within recessed

area 1006. It should be recognized that electropolishing can have a better control and therefore cause less process problems when trying to overpolish metal layer in recessed area 1006 as compare with wet etching method. For a description of electropolishing, see U.S Patent Application Serial No. 09/497,894, entitled METHODS AND APPARATUS FOR ELECTROPOLISHING METAL INTERCONNECTIONS ON SEMICONDUCTOR DEVICES, filed on February 4, 2000, which is incorporated in its entirety herein by reference.

Next, with reference to Fig. 2B, when as CF_4/O_2, SF_6/O_2, and the like, are added to the etching gases, Ta, C and F residue 2012 is formed on barrier layer 1004 and metal layer within recessed area 1006, with a more residue 2012 forming over and about recessed area 1006. As shown in Fig. 2C, when barrier layer 1004 is being etched away, the presence of residue 2012 can prevent barrier layer between dielectric material 1008 and deposited metal on the recessed area 1006 from been over-etched.

Additionally, the following table, Table 1, provides an exemplary range of parameters that can be employed in a plasma dry etch process to remove the barrier layer:

Table 1

Plasma Power:	500 to 2000 W
Vacuum:	30 to 100 mTorr
Temperature of wafer:	approximately 20° C
Gas and flow rate:	SF_6 = 50 sccm,
	CF_4 = 50 sccm, or
	O_2 = 10 sccm
Gas pressure:	0.1 to 50 mTorr
Removal rate of TaN:	250 nm/min
Removal rate of TiN:	300 nm/min
Removal rate of SiO_2:	200 ~ 400 nm/min

These parameters result in a removal rate of TaN and TiN, two possible barrier layer 1004 materials, close to that of SiO_2, a possible dielectric material 1008 material. The selectivity can be selected in this manner to reduce etching or damaging the underlying dielectric material 1008 during the removal of the barrier layer 1004. It should be noted, however, that other selectivity can be obtained by varying the parameters.

Now with reference to Fig. 2D, a portion of recessed area 1006 and non-recessed area 2014 of about Δd can be removed by using plasma etching process, or dry chemical cleaning, or any other convenient process. The etch rate of barrier layer 1004 should be set equal or lower than that of dielectric material 1008 in order to make sure the barrier layer 1004 is equal or higher than dielectric material 1008 in height. Therefore, no voids will be formed when the next top layer is deposited.

In Figs. 3A to 3D, another exemplary process is shown. The exemplary process shown in Figs. 3A to 3D is similar in many respects to the process shown in Figs. 2A to 2D, except that hard mask 3014 is deposited on dielectric material 1008 before wafer undergo etching and deposition processes that form recessed areas such as 1006. As shown, hard mask 3014 can prevent etching of dielectric material 1008 underneath of hard mask layer 3014 during barrier removal processes and therefore avoid the performance degradation of dielectrics, especially low-k dielectrics. Recess h should be less than the sum of thickness of barrier layer 1004 and the thickness of hard mask 3014.

In Figs. 4A to 4B, another exemplary process is shown. Like Figs. 3A to 3D, the exemplary process shown in Figs 4A to 4D is similar in many respects to the process shown in Figs. 2A to 2D, except that in addition to hard mask 3014, sacrificial layer 4016 is deposited on top of hard mask 3014. While hard mask layer 3014 has lower removal rate than that of barrier layer 1004, in this exemplary process, sacrificial layer with a removal rate equal or greater than that of barrier layer 1004 will be used.

In both Fig. 3 and Fig. 4, hard mask materials can be selected from SiN, SiC, SiO_2, and sacrificial layer can be selected from SiN and SiO_2.

Although the present invention has been described with respect to certain embodiments, examples, and applications, it will be apparent to those skilled in the art that various modifications and changes may be made without departing from the invention.

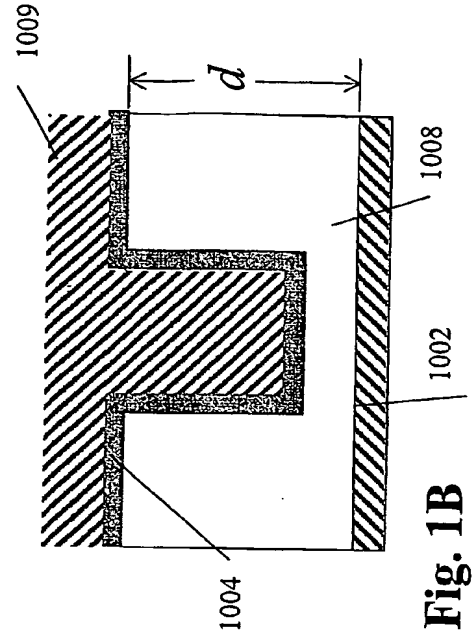

Fig. 1B

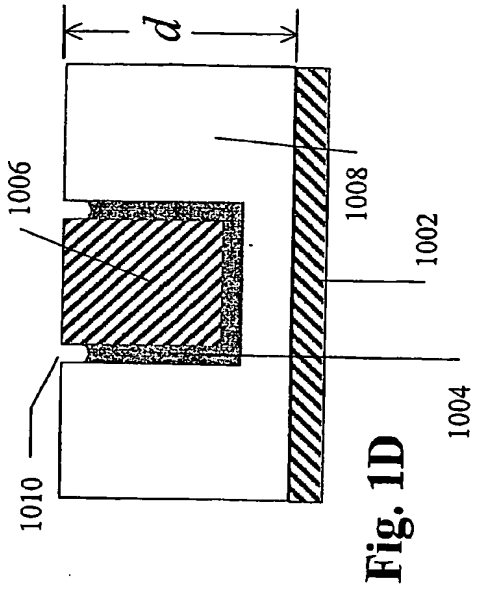

Fig. 1D

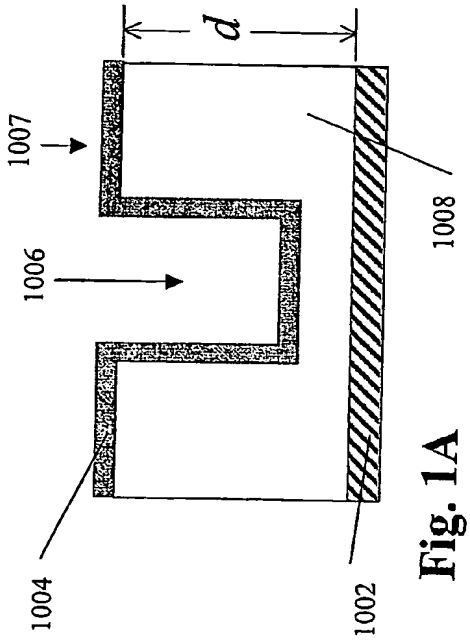

Fig. 1A

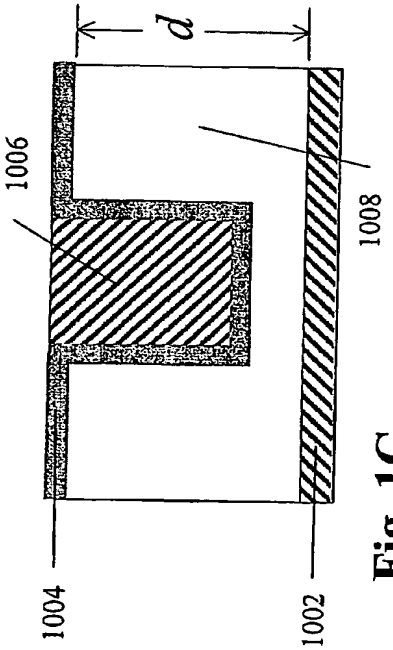

Fig. 1C

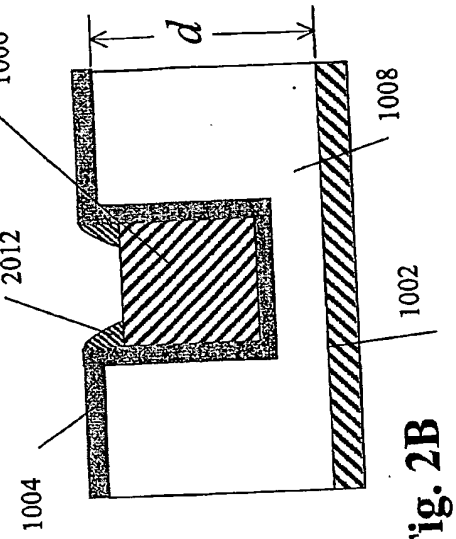

Fig. 2B

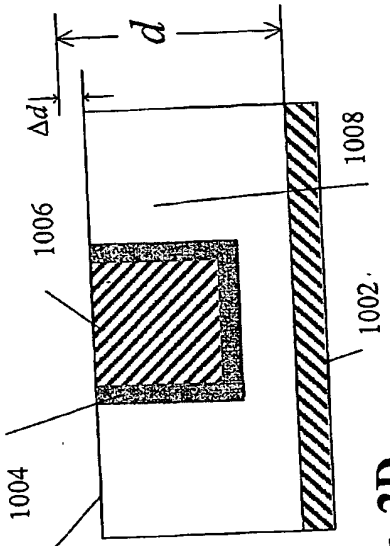

Fig. 2D

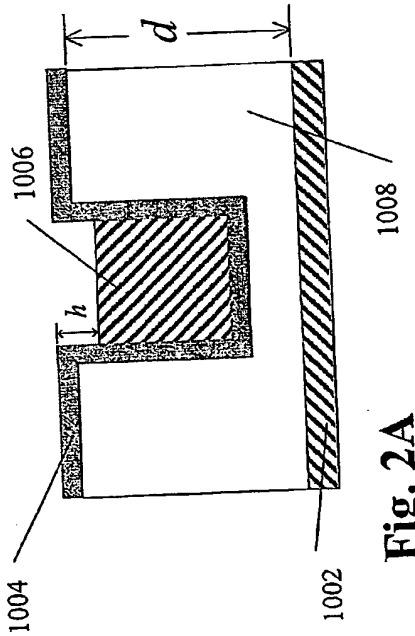

Fig. 2A

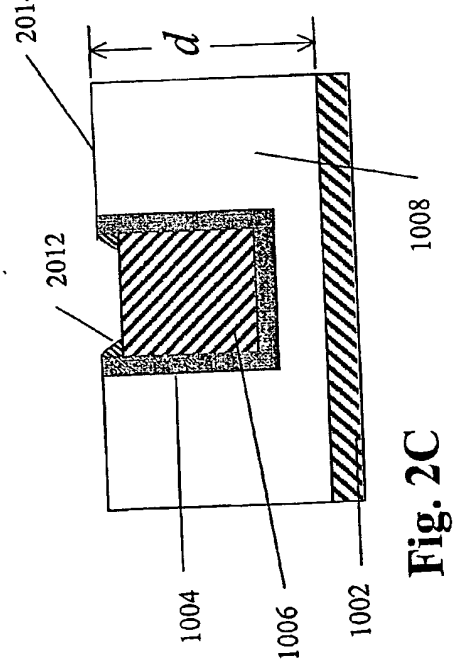

Fig. 2C

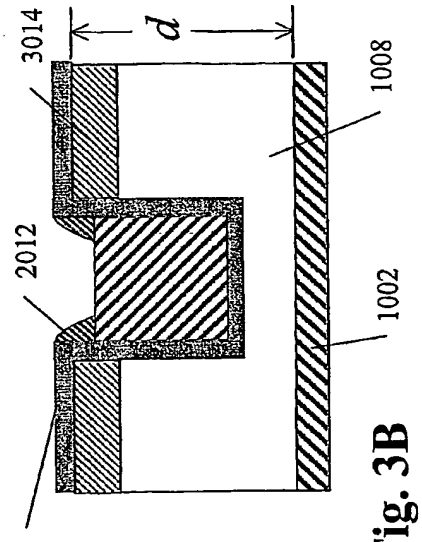

Fig. 3B

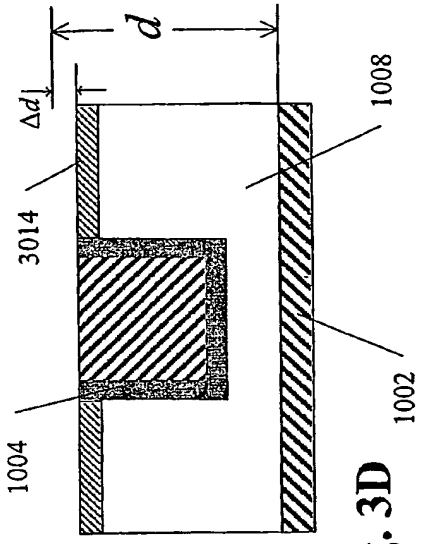

Fig. 3D

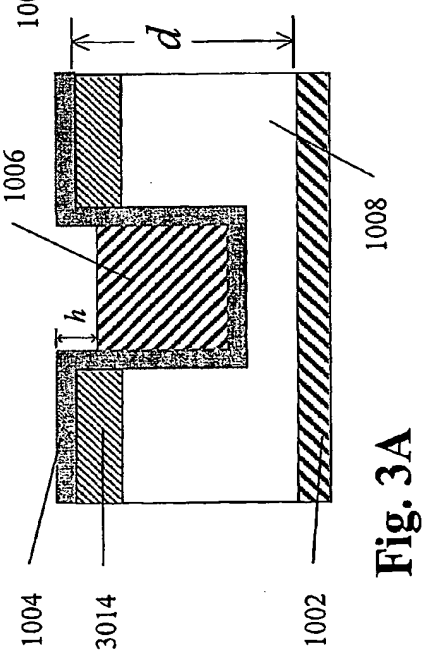

Fig. 3A

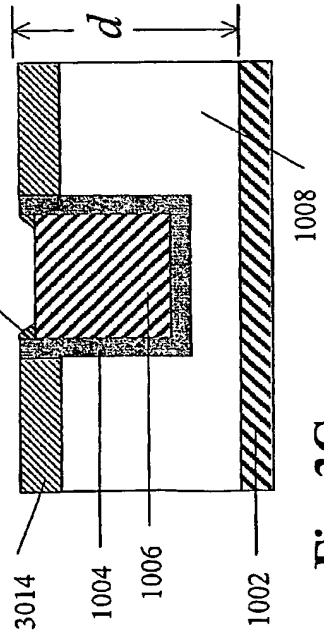

Fig. 3C

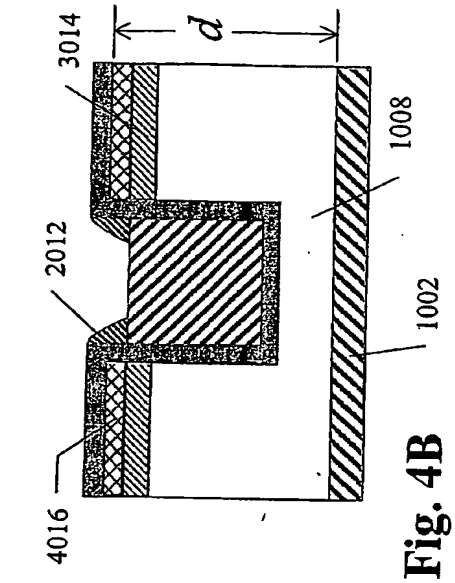

Fig. 4B

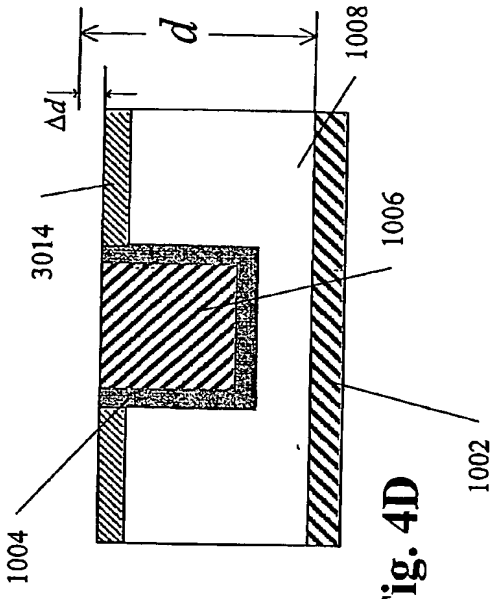

Fig. 4D

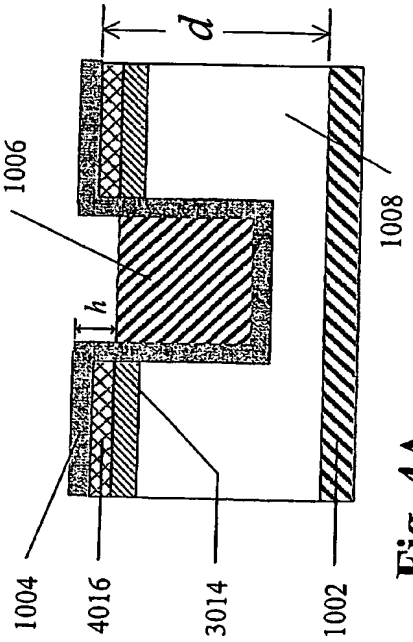

Fig. 4A

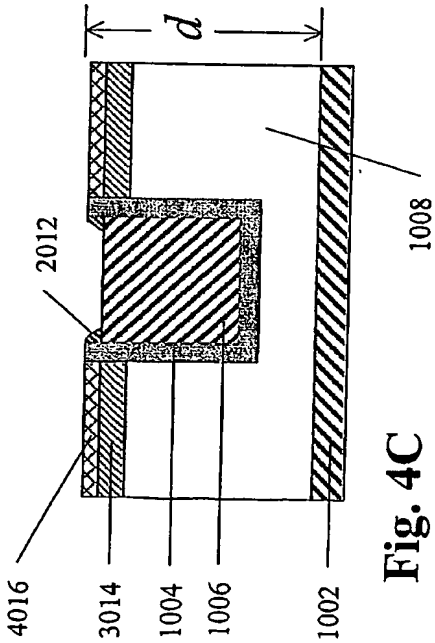

Fig. 4C

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